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Localizing trapped charge carriers in NO₂ sensors based on organic field-effect transistors

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Field-effect transistors have emerged as NO₂ sensors. The detection relies on trapping of accumulated electrons, leading to a shift of the threshold voltage. To determine the location of the trapped electrons we have delaminated different semiconductors from the transistors with adhesive tape and measured the surface potential of the revealed gate dielectric with scanning Kelvin probe microscopy. We unambiguously show that the trapped electrons are not located in the semiconductor but at the gate dielectric. The microscopic origin is discussed. Pinpointing the location paves the way to optimize the sensitivity of NO₂ field-effect sensors. © 2012 American Institute of Physics. [<http://dx.doi.org/10.1063/1.4758697>]

Nitrogen dioxide (NO₂) is a major air pollutant, which is released during the combustion of fossil fuels. This gas plays an important role in the formation of ozone, acid rain, and photochemical smog. Inhalation of NO₂ has been linked to adverse respiratory effects including airway inflammation in healthy people and to increased respiratory symptoms in people with asthma. The huge impact of NO₂ emission on public health and the environment has led to extensive scientific and technological progress in the field of NO₂ sensors.^{1,2} Many sensors are commercially available, such as electrochemical, resistive, and optical sensors.

Recently, field-effect transistors (FETs) have attracted attention as an alternative NO₂ sensing technology. A wide variety of semiconductors has been investigated, for example, amorphous organic semiconductors,³ carbon nanotubes,⁴ and metal oxide nanowires.⁵ In all cases, current changes upon NO₂ exposure have been demonstrated; i.e., a current decrease for *n*-type semiconductors and a current increase for *p*-type semiconductors. The current change is caused by a shift of the threshold voltage. This shift is due to fixed negative interface charges.⁶ Hence, electron trapping is the generic mechanism for NO₂ detection in field-effect transistors.

The dynamics of electron trapping in NO₂ sensors have been investigated for the model semiconductor ZnO.^{7,8} An important factor for the sensing in a field-effect transistor is the gate bias, which sets the electron density. Without applying a gate bias transistors are stable in NO₂ ambient. With a positive gate bias, however, electrons are accumulated that are getting trapped. At infinite time, all induced carriers have become immobile. Then the threshold voltage, here defined as the onset of current flow, is equal to the applied gate bias.

The NO₂ concentration determines the charge trapping dynamics. The characteristic time for charge trapping is found to be inversely proportional to the NO₂ concentration.⁷

Despite many investigations on the mechanism of NO₂ detection with field-effect transistors the actual location of the trapped charges has remained unresolved. The electron trapping can be either in the bulk of the semiconductor or at the interface between the semiconductor and the gate dielectric. The exact location cannot easily be determined because the gate dielectric interface is buried under the semiconductor. Here, we used the very simple but effective technique of exfoliating the semiconductor with adhesive tape. The revealed gate dielectric is then accessible for characterization with scanning Kelvin probe microscopy (SKPM).^{9,10} This technique was earlier applied to reveal the location of trapped charges due to gate bias stress¹¹ and to link the threshold voltage shift in a transistor with a SAM-modified gate dielectric to charges trapped by the SAM.¹²

To apply the exfoliation technique, we choose organic semiconductors. Using adhesive tape they can be completely removed at once. The transistors were charged by applying a gate bias in an NO₂ ambient. *In situ* measurements of the surface potential within the transistor channel were performed before and after exfoliation, using SKPM measurements. Comparison of the obtained surface potentials with and without the semiconductor present did pinpoint the location of the trapped electrons at the gate dielectric interface. The location could be confirmed by using a variety of organic semiconductors.

Field-effect transistors were prepared on heavily doped Si wafers acting as common gate. A 200 nm thermally grown SiO₂ layer was used as bottom gate dielectric. Gold source and drain contacts with a thickness of 30 nm were defined by conventional photolithography, resulting in finger transistors with a channel length and width of 10 and 10 000 μm,

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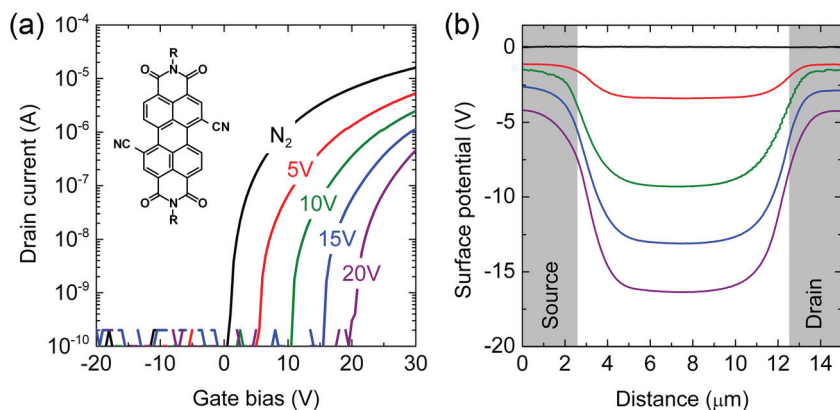


FIG. 1. Charge carrier trapping in NO_2 ambient. (a) Transfer curves of a field-effect transistor using as a semiconductor ActivInk N1400 blended with polystyrene. The gate sweep was recorded at a source-drain bias of 10 V. The black transfer curve corresponds to the pristine transistor in N_2 . The transistor was then exposed to 1.5 ppm NO_2 and measured after application of a positive gate bias of the indicated value for 60 s. The threshold voltage shifts to the applied gate bias. The inset shows the chemical structure of ActivInk N1400. (b) Potential profiles corresponding to the transfer curves of Figure 1(a) with ActivInk N1400 still present.

respectively. A 2 nm Ti layer was used as an adhesion layer for the contacts. To reduce gate bias stress and to facilitate the exfoliation process, the gate dielectric was passivated with vapor deposited hexamethyldisilazane (HMDS).

As a semiconductor we use a *N,N*-dialkylsubstituted-(1,7&1,6)-dicyanoperylene-3,4,9,10-bis(dicarboximide) derivative (Polyera ActivInkTM N1400), a well-established air-stable *n*-type semiconductor that exhibits charge carrier mobilities of 0.01–0.4 cm^2/Vs . The chemical structure is given as inset in Figure 1(a). The semiconductor was blended with high molecular weight polystyrene (M_w 994 000 g/mol, Aldrich Chem. Co.). This high molecular weight polymer provides mechanical robustness to the film for improved exfoliation while the device performance is not compromised, as shown in recent studies on solution blending of organic semiconductors with organic insulating polymers.^{13–17} Thin films were made by spin coating a blend containing 3.6 mg/ml of ActivInk N1400, filtered with a 5 μm filter, and 18 mg/ml polystyrene in chloroform. The perylene bisimide films were annealed in vacuum at 110 $^\circ\text{C}$ for 1 h to remove residual water and solvents.

Electrical characterization of the blend was performed under vacuum using an HP 4155B semiconductor parameter analyzer. The extracted mobility was about 0.02 cm^2/Vs , and the current modulation was over 4 decades, similar to the specifications of the pure ActivInk N1400. Gas measurements were performed in a Teflon flow chamber equipped with feed-throughs for electrical contacting. NO_2 was supplied from a cylinder containing 3 ppm NO_2 in the carrier gas N_2 (Praxair). Additional nitrogen was used to further dilute the mixture. The concentration was regulated using two mass flow controllers.

First we study the charge trapping caused by NO_2 in perylene bisimide transistors with the semiconductor still present. The pristine transistor in N_2 exhibits a 0 V threshold voltage, shown as the black transfer curve in Figure 1(a). The transistors were then exposed to 1.5 ppm NO_2 and subjected for 60 s to a continuous gate bias of 5, 10, 15, or 20 V, while the source and drain electrodes were grounded. Transfer characteristics measured directly after the charge trapping are presented in Figure 1(a). The threshold voltage has shifted completely to the applied gate bias after 60 s, indicating that all free charge carriers have been trapped. As a reference, a transistor was stressed without NO_2 for 60 s by applying a gate bias of 20 V. The resulting threshold voltage shift was then only 0.5 V. This small value rules out conven-

tional gate bias stress as a cause for the threshold voltage shift on these time scales.

The charged transistors were analyzed with SKPM as quickly as possible after measuring the transfer curves, allowing for a direct measurement of the surface potential. During the SKPM measurement, all electrodes were grounded. We note that perylene bisimide is a unipolar *n*-type semiconductor that does not support holes. Therefore the bulk perylene bisimide semiconductor cannot screen negative charges in the channel and SKPM can be used to visualize trapped negative charges. The local surface potentials in the channel are presented in Figure 1(b). The pristine transistor with a 0 V threshold voltage shows a surface potential of around 0 V, which indicates that there are no immobile charges present. The values of the surface potentials measured in the channel of the charged transistors are negative and in correspondence with the value of threshold voltage. The good agreement indicates that the origin of the threshold voltage shift is trapped charges. We note that the slight deviation originates from the finite spatial resolution of the SKPM system¹⁸ and a decrease of the amplitude of the surface potential with time, especially in light. Starting the potential profile measurement after determining the threshold voltage takes about one minute. The nonzero potential measured on top of the source and drain contacts is again due to the spatial resolution.

SKPM does not distinguish between electrons trapped in the bulk perylene bisimide semiconductor or at the gate dielectric interface. The experiment to find the exact location of the trapped charges is schematically depicted in Figure 2. The transistor with the trapped electrons exhibits a positive threshold voltage. The trapped charges are either in the semiconductor (I) or at the dielectric (II). In both cases, because there is no screening by the unipolar bulk *n*-type semiconductor, the trapped charges give rise to a negative surface potential with a magnitude equal to the value of the threshold voltage shift. A distinction can be made after exfoliation of the semiconductor. In case I, the exfoliation will remove the semiconductor including the trapped charge carriers. The resulting surface potential is then zero. In case II, the trapped charges will stay behind at the dielectric, and a negative surface potential remains.

An N1400 ActivInk transistor is exposed to NO_2 and a gate bias of 20 V is applied for 60 s. The surface potential, measured as quickly as possible after charge trapping, is presented as the black curve in Figure 3(a). The negative surface

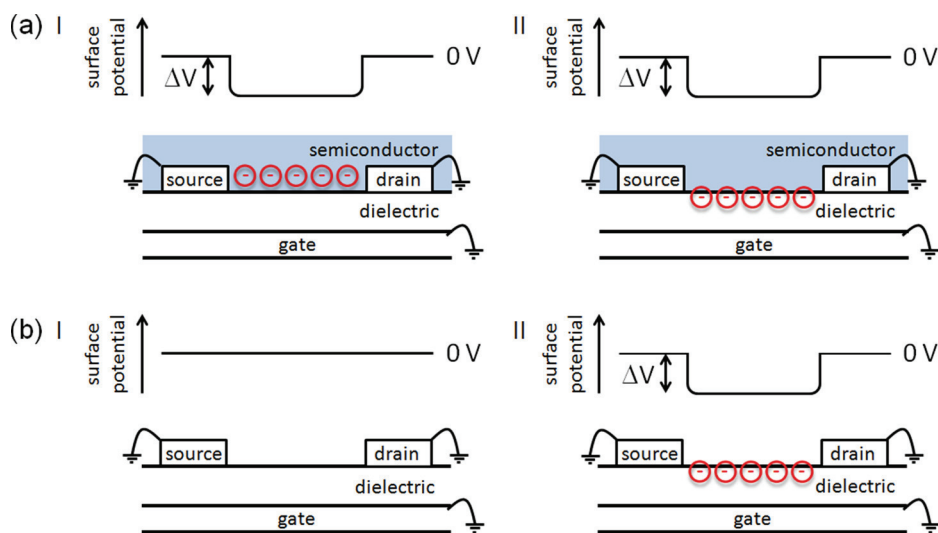


FIG. 2. Schematic of the exfoliation experiment to localize trapped charge carriers. (a) The transistor after applying a positive gate bias in NO_2 . The trapped charges are either in the semiconductor (I) or at the interface with the gate dielectric (II). In both cases, when there is no screening, the trapped charges give rise to a negative surface potential equal to the threshold voltage shift, ΔV . (b) Transfer characteristics after the exfoliation process. In case I, the exfoliation will remove the semiconductor including the trapped charge carriers. The resulting surface potential is then zero. In case II, the trapped charges will stay behind at the gate dielectric interface and the negative surface potential remains.

potential indicates the presence of trapped charges. To locate the charges, the experiment was repeated and the exfoliation technique was applied. The transistor is exposed to NO_2 using the same charge trapping procedure. However, now the semiconductor is delaminated after stressing using adhesive tape and tweezers, as shown in Figure 3(b). The exposed gate dielectric is probed with SKPM. The potential profile after exfoliation is shown as the red curve. The surface potentials are similar with and without semiconductor, which demonstrates that the charges are not trapped in the semiconductor but trapped at the gate dielectric interface. The minor differences are due to recovery in ambient light before the SKPM measurement starts, when the semiconductor is still present.

We note that it is well-known that exfoliation of two insulating materials can yield static charges by contact electrification or tribo-charging. However, as discussed previously¹² the potentials measured here are not generated by the peeling process. First the measured potentials are reproducible, and second, the correspondence of the threshold voltage shift with the surface potential would be a rare coincidence.

The clear contrast in the optical photograph of Figure 3(b) shows that the exfoliation is almost complete. Investigation with AFM showed only minute residues, due to the phase separation between polystyrene and perylene bisimide.¹⁹ The almost complete delamination is confirmed by photo-excitation experiments. With the semiconductor still present the surface potential and the threshold voltage are recovered by turning on the light of the microscope. In this case the trapped charges are released. However, after delamination the surface potential does not change. The photo-excited carriers cannot percolate to the contacts; the surface charges remain trapped.

To support the assignment of trapped charges to the gate dielectric we repeated the experiments with two other semiconductors, viz., poly(perylen bisimide acrylate) (PPerAcr, M_w 30 900 g/mol, PDI 1.86) and polytriarylamine (PTAA). Both semiconductors can be completely removed by stripping. The chemical structures are presented in the insets of Figure 4. The synthesis and properties of PPerAcr have been described previously.^{20,21} Thin films were spincoated from a 5 mg/ml solution in chloroform and annealed for one hour at

210 °C. Field-effect transistors showed unipolar n -type characteristics with a mobility of about $4 \times 10^{-4} \text{ cm}^2/\text{Vs}$. The threshold voltage shifted upon application of a gate bias in an NO_2 ambient. The kinetics was comparable to that of the low molecular weight perylene bisimide. The surface potentials before and after exfoliation are presented in Figure 4(a). When the semiconductor is still present a large negative surface potential is measured. Because PPerAcr is a unipolar n -type semiconductor the trapped charges again cannot be screened. The surface potentials before and after exfoliation are similar confirming that the charges are trapped at the gate dielectric interface.

The experiments were repeated using PTAA, a well-established air-stable unipolar p -type semiconductor that exhibits charge carrier mobilities of 10^{-3} to $10^{-2} \text{ cm}^2/\text{Vs}$.²² In an NO_2 ambient the threshold voltage of a PTAA transistor shifts towards the applied positive gate bias. The sign of the shift indicates the presence of trapped electrons. We note that the barrier for electron injection into PTAA is too large to inject electrons within the time scale of the experiments.²³ The presence of the electrons could be due to surface

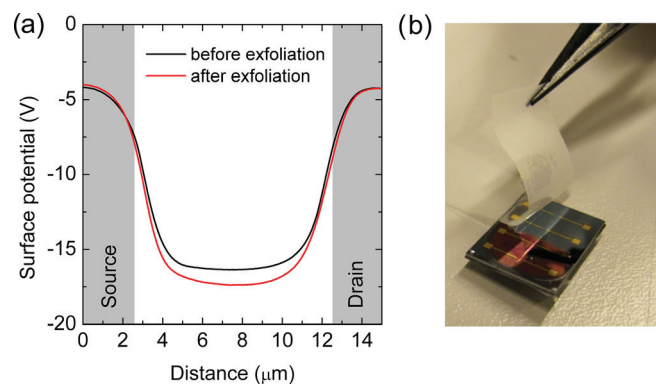


FIG. 3. Comparison of surface potential before and after delamination. (a) Surface potential profiles of an N1400 ActivInk transistor after applying a 20 V gate bias for 60 s in NO_2 . The black curve shows the potential profile with the semiconductor still present and the red curve shows the potential profile after delamination. The surface potentials are identical both with and without semiconductor, which demonstrates that the charges are not trapped in the semiconductor but trapped at the gate dielectric interface. (b) The actual exfoliation process, using adhesive tape and tweezers.

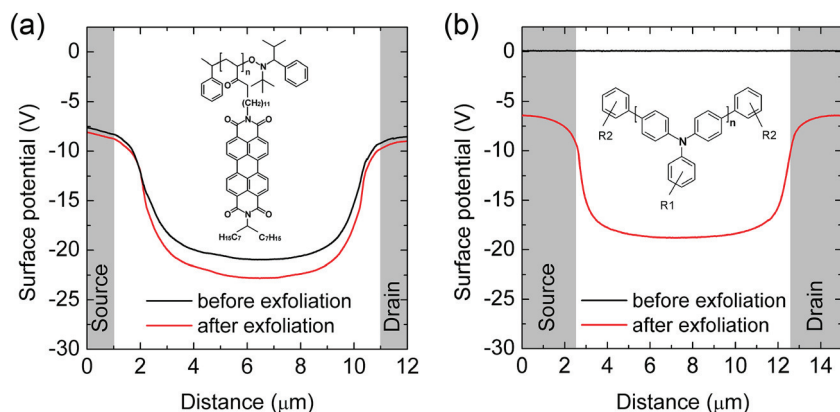


FIG. 4. Exfoliation of different semiconductors. (a) Surface potential profiles of *n*-type poly(erylene bisimide acrylate) (PPerAcr) field-effect transistor after applying a gate bias of 30 V for 60 s in NO₂. The chemical structure of PPerAcr is shown in the inset. The black curve shows the potential profile with the semiconductor still present and the red curve shows the potential profile after delamination. (b) Surface potential profiles of a *p*-type PTAA field-effect transistor, after applying a gate bias of 20 V for 300 s in NO₂. The chemical structure of PTAA is shown in the inset. The black curve shows the potential profile with the semiconductor still present and the red curve shows the potential profile after delamination.

conduction of the SiO₂ gate dielectric,²⁴ but the origin is not completely clear. Subsequently the surface potentials of the stressed transistor were measured before and after exfoliation. Figure 4(b) shows that the surface potential with the PTAA semiconductor still present is about 0 V throughout the channel. The trapped electrons did not appear in the surface potential as they were screened by mobile holes in the *p*-type PTAA semiconductor. However, the trapped electrons were clearly visible as a large negative surface potential after peeling off the PTAA semiconductor. For both PPerAcr and PTAA AFM measurements showed that the semiconductor was completely removed by exfoliation. The magnitude of the surface potential showed a good agreement with the threshold voltage shift, pointing to electron trapping. SKPM measurements after exfoliation revealed that the trapped electrons are located at the gate dielectric.

The microscopic mechanism of the charge trapping remains unknown. It is different from that in commercially available chemiresistors. When the resistor is exposed to NO₂, the NO₂ adsorbs on the surface of the metal oxide and redox reactions take place.¹ The extraction of electrons from the metal oxide results in an increase in the width of the depletion layer and of the corresponding potential barriers at the grain boundaries. Then the resistance increases, or the current decreases. Transistors, however, are stable in NO₂ without applying a gate bias. The source-drain current only changes when a positive gate bias is applied, i.e., when electrons are accumulated. The origin is a shift in threshold voltage due to trapped charges at the gate dielectric and not due to a change in grain boundary resistance.

The detection mechanism in a transistor cannot simply be trapping of an electron by an isolated NO₂ molecule as might be expected from the large electronegativity of NO₂. This reduction process should take place no matter if the NO₂ molecule is in the bulk of the semiconductor or at the gate dielectric interface. However, the exfoliation experiments presented here have unambiguously shown that the trapped electrons are located at the gate dielectric. Furthermore, the literature data show that the type of semiconductor does not play a role.^{3–5} Current changes upon NO₂ exposure for a wide variety of semiconductors have been reported. Finally for the three semiconductors investigated here, the charge trapping dynamics are comparable. Apparently not the type of semiconductor but the nature of the gate dielectric is crucial. Here we use SiO₂ passivated with HMDS. Pre-

liminary experiments have shown that the trapping time may increase when the HMDS coverage increases. Experiments with organic gate dielectrics were inconclusive as the semiconductor could not selectively be delaminated. The use of various dielectrics to identify the microscopic nature of the trap is a topic of further research.

In summary, field-effect transistors have emerged as NO₂ sensors. When applying a positive gate bias, electrons accumulated in the channel are getting trapped. At infinite time, all induced charge carriers are immobile, leading to a threshold voltage equal to the applied gate bias. To determine the location of the trapped electrons we have delaminated the semiconductor with adhesive tape and measured the surface potential of the revealed gate dielectric with scanning Kelvin probe microscopy. The exfoliation technique can be utilized because the semiconductor is bound by weak van der Waals forces. Three different organic semiconductors have been used. The exfoliation experiments have unambiguously shown that the trapped electrons are located not in the semiconductor but at the gate dielectric, here SiO₂. Pinpointing the location paves the way to optimize the sensitivity of NO₂ field-effect sensors.

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